REMARKS

The Office Action dated August 16, 2004 has been fully considered by the Applicant. Claims 1, 7, 11 and 14 have been currently amended. Claims 2-6, 8-10, 12-13 and 15-16 have been previously presented.

Enclosed is a Petition for Three-Month Extension of Time and a check in the amount of $1020 to cover the cost of the Petition.

Also attached is an Information Disclosure Statement listing the cited references found in a search conducted in the corresponding European patent application. The Search was conducted on 26 November 2004. Copies of the patents found in the search are also enclosed.

The title has been amended to be more descriptive as requested by Examiner Kostak.

Claim 14 has been objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Claim 14 has been currently amended to overcome the objection.

Claims 1-16 have been rejected under 35 USC 103(a) as being unpatentable over United States Patent No. 4,412,244 to Shanley, II in view of United States Patent No. 4,218,698 to Bart et al. Independent claims 1, 7, and 11 have been currently amended to include that the video data amplifier and driver circuit is adaptable when operating in response to changes in the supply voltage and other environmental conditions in which the broadcast data receiver operates and compensates for the changes in the supply voltage and other environmental condition via generation of a level of DC offset on an input transistor of the video data amplifier and driver circuit, the DC offset value is added tot he video data signal to form a combined signal. Neither the '244 Shanley II patent or the '698 patent teach of a video data amplifier and driver circuit that when operational is adaptable

in response to change in a supply voltage and other environmental conditions. Therefore, Applicant respectfully requests reconsideration of the rejection.

The final output voltage of '244 patent is not immune to supply voltage change. The '244 patent is directed toward superimposing graphics on a black and white signal wherein the contrast ratio of the graphics can be adjusted by adjusting the DC level. The '244 document discloses that the "color signal is developed in the collector output circuit of transistor 32' (see col. 2, lines 36-38) and, as such, there is no compensation for supply voltage Vcc variation. Furthermore, the signal in the '244 patent is supplied to the drive "by means of a coupling network comprising a plurality of cascade connected emitter follower transistors 40, 41, and 42" (see Col 3, lines 38-40). In the '244 patent there is no gain in this part of the circuit, and temperature variations are compensated by careful calibration of the opposite polarity transistors 40 and 41. Therefore, Applicant sincerely believes that the claims as currently amended are novel over the '244 Shanley II patent and therefore requests reconsideration of the rejection.

In the '698 patent to Bart et al, "the graphics only" portion of the circuit (from transistor 71 through to diodes 70 and 80) set voltages which do not compensate for changes in the supply voltages, as does Applicant's invention, because they are obtained by potential divider resistor networks across the supply. Further, the '698 patent to Bart et al is directed toward a peak holding circuit rather than a video amplification circuit, controlling voltage levels to determine the graphics display intensity level. The '698 Bart et all transistors 50, 57 and 60 form a low frequency peak holding circuit with no voltage gain. In contrast to Applicant's invention, the '698 Bart et al circuit cannot work down to zero input voltage because of transistor 50's emitter base offset. Therefore, Applicant's believe that the claims as currently amended are novel over the '698 Bart et al patent and respectfully request reconsideration of the rejection.

In summary, is it clear that neither the "698 Bart et al patent or the '244 Shanley, II patent compensates for changes in the supply voltage and other environmental conditions via generation of a level of DC offset on an input transistor of the video data amplifier and driver circuit and adding the DC offset value to the video signal to form a combined signal. Applicant respectfully requests reconsideration of the rejection.

It is believed that the application is now in condition for allowance and such action is earnestly solicited. If any further issues remain, a telephone conference with the Examiner is respectfully requested. If any fees are associated with this response, please charge Deposit Account No. 08-1500.

Respectfully Submitted

HEAD, JOHNSON & KACHIGIAN

Dated: 16 Feb. 2005

BY: _____

Mark G. Kachigian, Reg. No. 32,840
228 West 17th Place
Tulsa, Oklahoma 74119
(918) 587-2000
Attorneys for Applicant